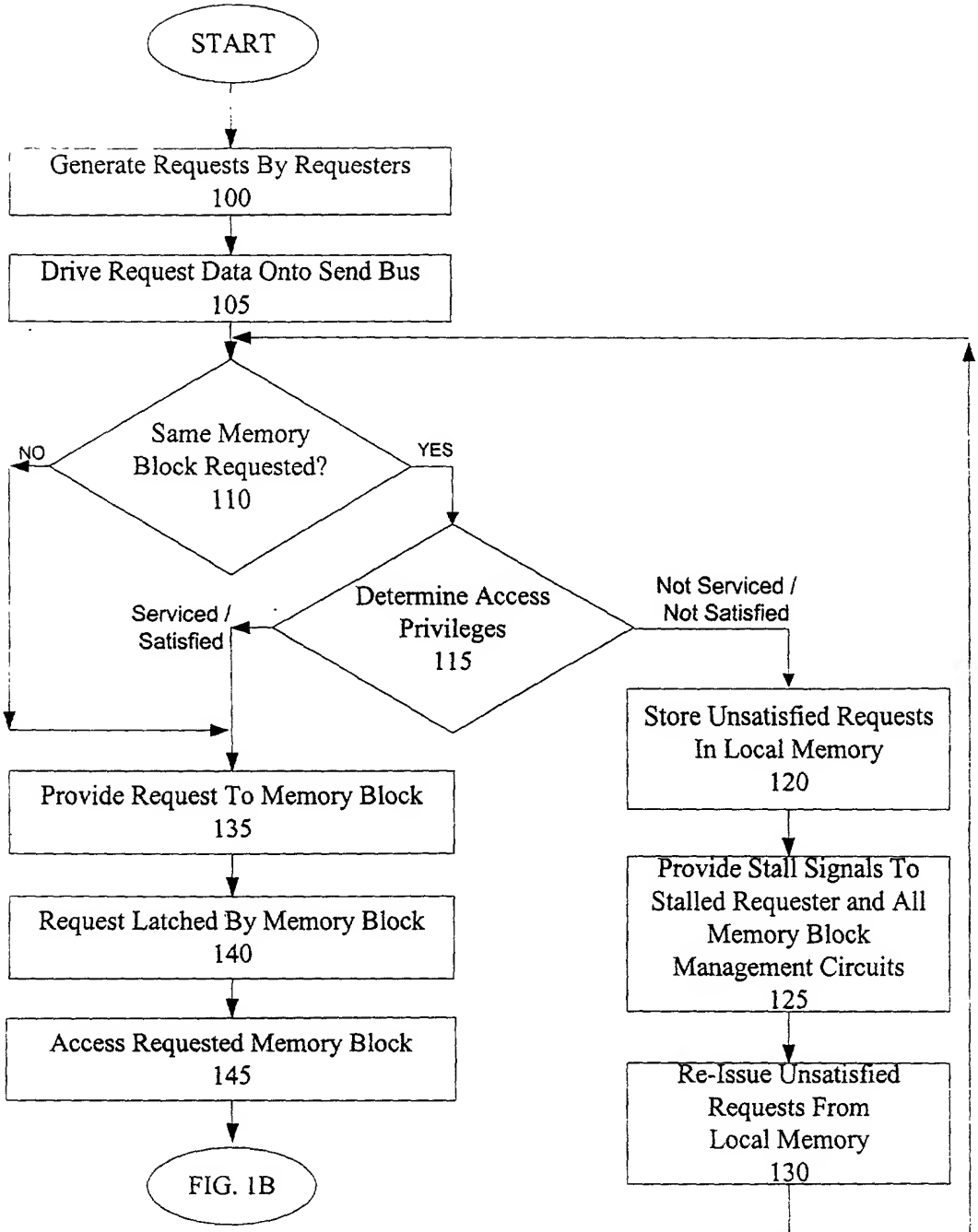

START
Generate Requests By Requesters 100
Drive Request Data Onto Send Bus 105
Same Memory Block Requested? 110
NO
YES
Determine Access Privileges 115
Serviced / Satisfied
Not Serviced / Not Satisfied
Store Unsatisfied Requests In Local Memory 120
Provide Stall Signals To Stalled Requester and All Memory Block Management Circuits 125
Re-Issue Unsatisfied Requests From Local Memory 130
Provide Request To Memory Block 135
Request Latched By Memory Block 140
Access Requested Memory Block 145
FIG. 1B

FIG. 1A

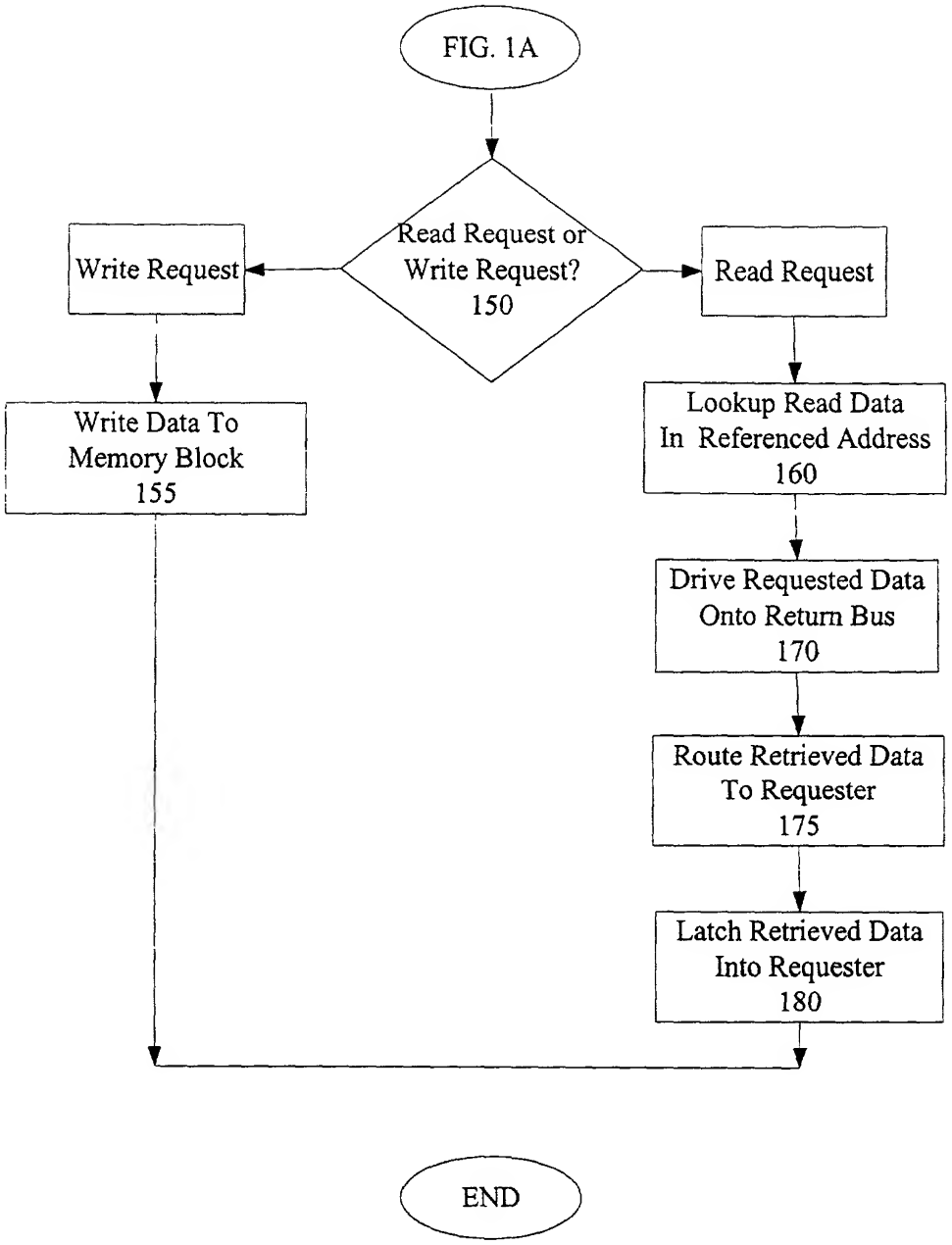
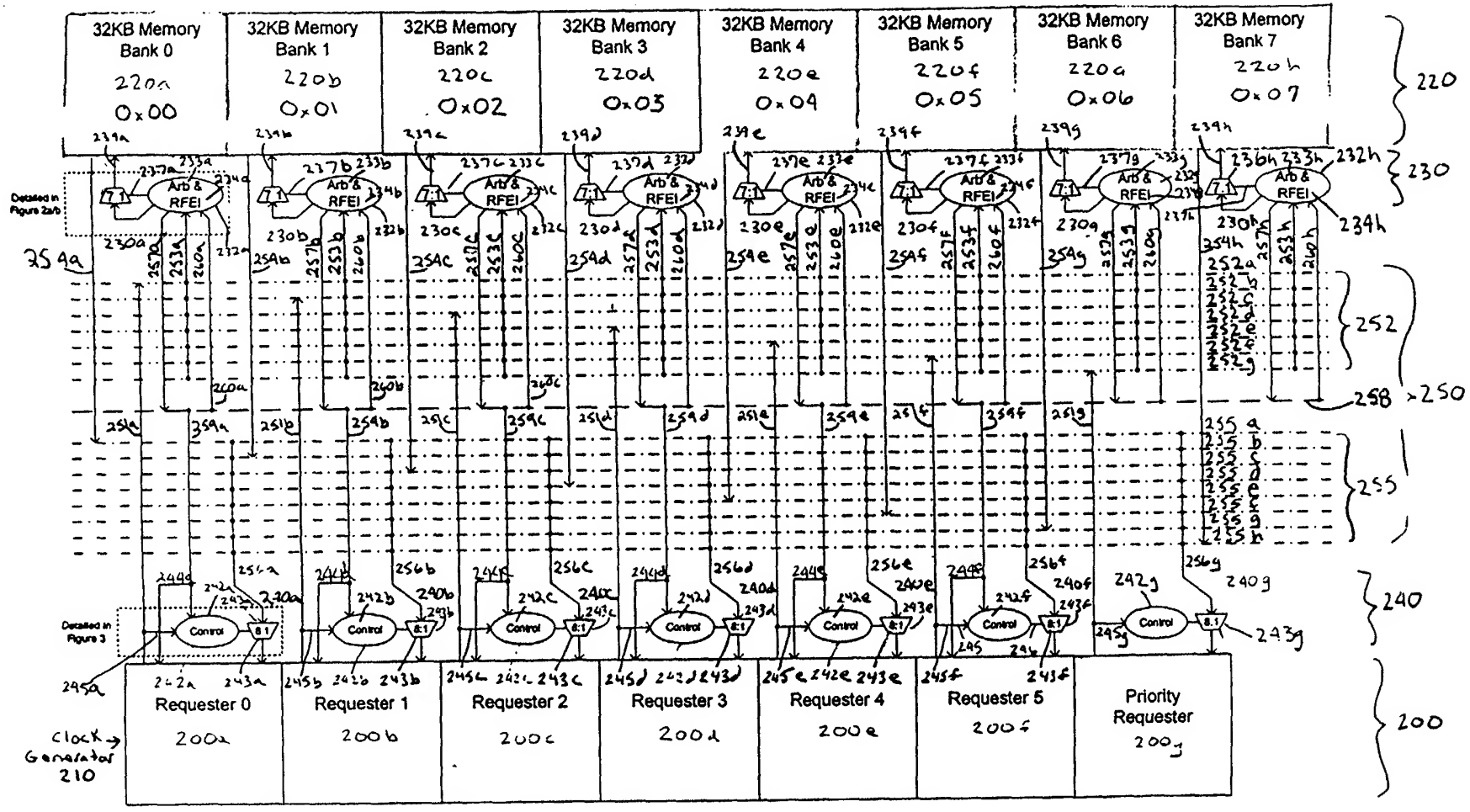


FIG. 1A
Read Request or Write Request? 150
Write Request
Read Request
Write Data To Memory Block 155
Lookup Read Data In Referenced Address 160
Drive Requested Data Onto Return Bus 170
Route Retrieved Data To Requester 175
Latch Retrieved Data Into Requester 180
END

FIG. 1B



Key:
- Request Bus: <req>CMValid, <req>CMAddr[15:0], <req>CMWrData[31:0], <req>CMBE[3:0], <req>CMReadNotWrite
- Stall Busses: c<req>IntStall[7:0] (Eight lines per requester - one driven by each bank).
- Data Return Bus: c<req>IntRdData[31:0]

Fig. 2

Attorney: Craig A. Gelfound
Docket No.: 42112/CAG/B600
Inventor(s): Lawrence J. Madar, III et al
Title: PIPELINED MULTI-ACCESS MEMORY APPARATUS AND METHOD
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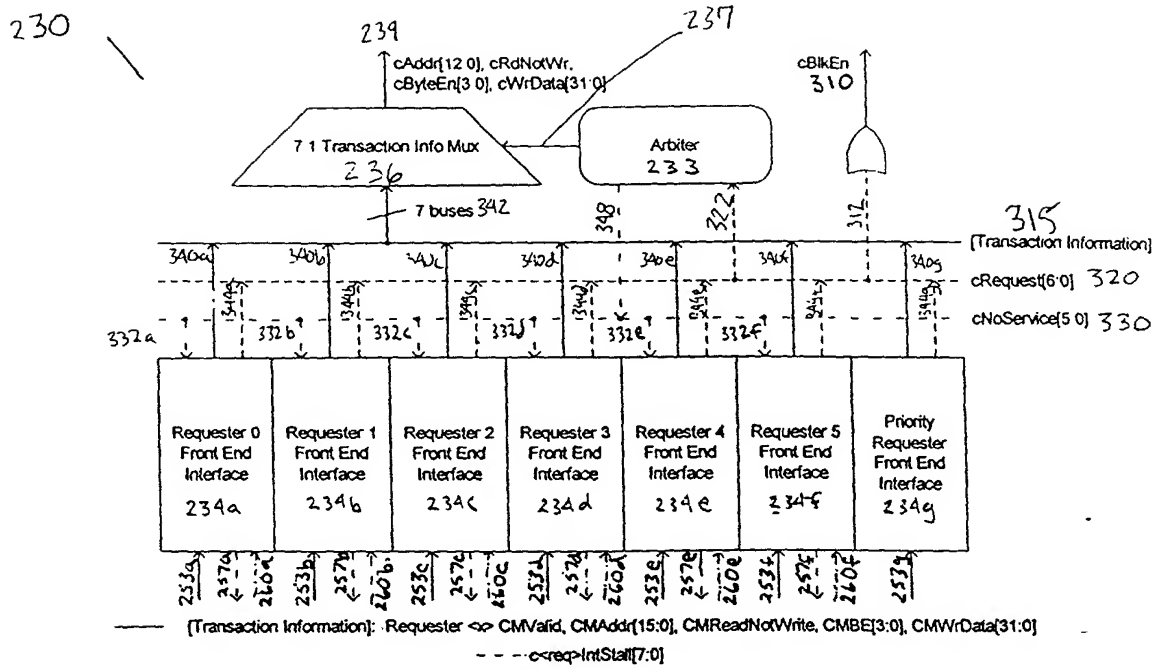
230
239
237
cAddr[12:0], cRdNotWr, cByteEn[3:0], cWrData[31:0]
cBlkEn
310
7:1 Transaction Info Mux
236
Arbiter
233
7 buses 342
348
322
312
315
[Transaction Information]
cRequest[6:0] 320
cNoService[5:0] 330
Requester 0 Front End Interface 234a
Requester 1 Front End Interface 234b
Requester 2 Front End Interface 234c
Requester 3 Front End Interface 234d
Requester 4 Front End Interface 234e
Requester 5 Front End Interface 234f
Priority Requester Front End Interface 234g
[Transaction Information]: Requester <x> CMValid, CMAddr[15:0], CMReadNotWrite, CMBE[3:0], CMWrData[31:0]
c<req>IntStall[7:0]

Fig.3

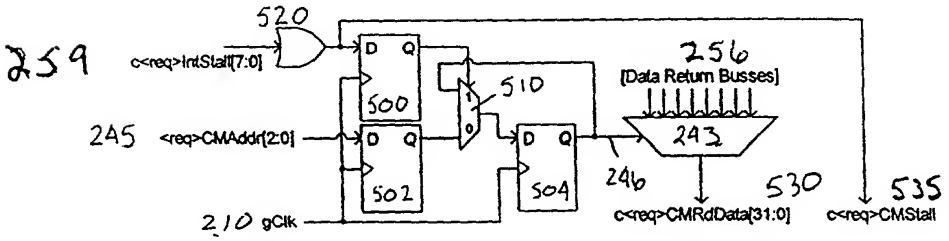
259
520
c<req>IntStall[7:0]
245
<req>CMAddr[2:0]
210 gClk
500
502
504
510
256
[Data Return Busses]
243
246
530
535
c<req>CMRdData[31:0]
c<req>CMStall

Fig.5

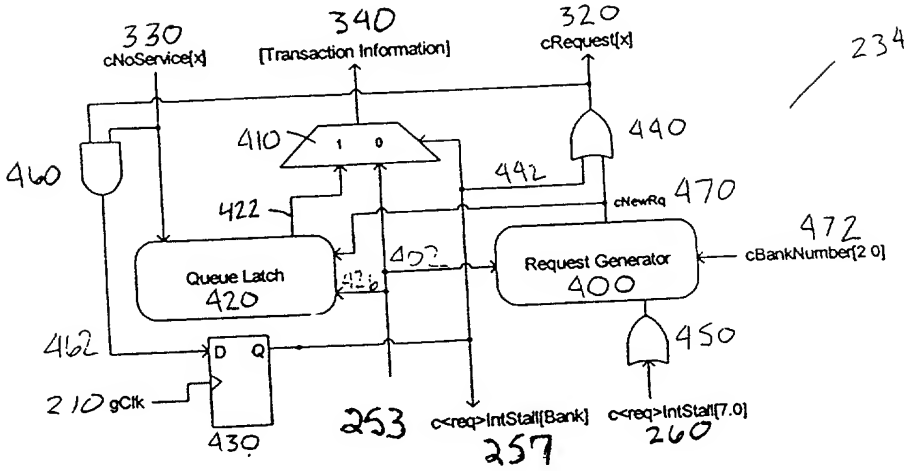
330
cNoService[x]
340
[Transaction Information]
320
cRequest[x]
234
410
1
0
440
460
442
422
cNewRq
470
472
Queue Latch
420
402
Request Generator
400
cBankNumber[2 0]
462
450
D
Q
210 gClk
430
253
c<req>IntStall[Bank]
257
c<req>IntStall[7.0]
260

Fig. 4

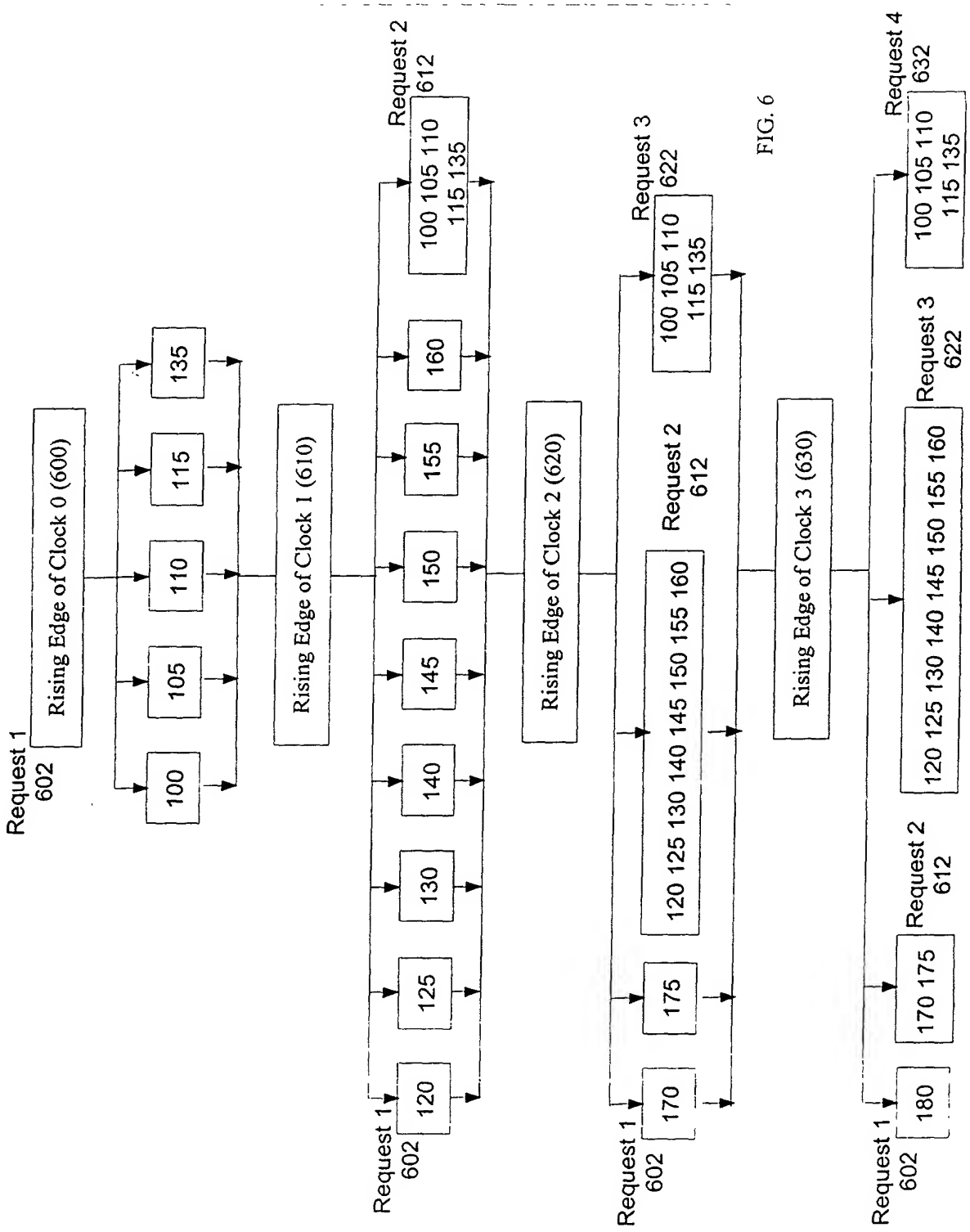
Request 1
602
Rising Edge of Clock 0 (600)
100
105
110
115
135
Rising Edge of Clock 1 (610)
Request 1
602
120
125
130
140
145
150
155
160
Request 2
612
100 105 110
115 135
Rising Edge of Clock 2 (620)
Request 1
602
170
175
120 125 130 140 145 150 155 160
Request 2
612
100 105 110
115 135
Request 3
622
Rising Edge of Clock 3 (630)
Request 1
602
180
170 175
Request 2
612
120 125 130 140 145 150 155 160
Request 3
622
100 105 110
115 135
Request 4
632

FIG. 6